AMENDMENTS TO THE CLAIMS

Claims 1-26. (Canceled)

27. (New) A processor comprising:

a CPU which has an operation state and a stop state, in the operation state the CPU operates in accordance with a clock, in the stop state the CPU stops operating in accordance with the clock,

wherein when the CPU is in the stop state, another processor is capable to be inputted data and store the data in a memory without making a transition from the stop state to the operation state in the CPU,

wherein when the CPU is in the operation state, the CPU is capable to process the data which is inputted and stored by the another processor while the CPU is in the stop state,

wherein the transition from the stop state to the operation state is independent of inputting the data to the another processor.

28. (New) A data apparatus comprising:

a block having a memory; and

a second processor which has an operation state and a stop state, in the operation state the second processor operates in accordance with a clock, in the stop state the second processor stops operating in accordance with the clock,

wherein when the second processor is in the stop state, the block is capable to be inputted data and store the data in the memory without making a transition from the stop state to the operation state in the second processor,

wherein when the second processor is in the operation state, the second processor is capable to process the data which is inputted and stored by the block while the second processor is in the stop state,

wherein the transition from the stop state to the operation state is independent of inputting the data to the block.